Graphene-enabled hybrid architectures for multiprocessors: bridging nanophotonics and nanoscale wireless communication

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ABSTRACT
Due to their out-standing performance (huge bandwidth and high signal quality), optical communications have become the standardized technologies suited for long reach and high bit-rate communication systems. Nevertheless, the traditional incompatibility of CMOS with the optical technology, and the difficulty for all-optical implementation of some key functions such as buffering and header processing, have been hindering the application of optical communications for short-range communications. However, the advent of nanophotonics is paving the way for such approach by enabling CMOS compatibility and the possibility of building out micro- and nanoscale optical components. In this paper, we do a first overview of the state-of-the-art in graphene and silicon nanophotonics, and its utilization for on-chip communication in multicore processors, to then propose a hybrid wireless/optical-wired architecture based on both a photonic Network-on-Chip (NoC) and a wireless NoC. The former for transferring heavy flows of data, the latter for supporting the control plane of the whole network, and carrying light data flows.
Keywords: Nanophotonics; Silicon-on-Insulator; Graphene; Plasmonics; Network-on-Chip; Hybrid

1. INTRODUCTION

Optical communications have been traditionally suited for high datarate transmission over medium and long distances, due to its high bandwidth density and its excellent properties in terms of attenuation and interference.

While such conditions would be also desirable for short range multihop communications, the employment of optical schemes in these cases has been regarded inefficient when compared to other wireline or wireless options mainly due to two reasons. First, optical technologies have been traditionally incompatible with standard CMOS processes, making the integration of optical components dependant on higher cost hybrid semiconductor integration techniques. Second and since optoelectric conversions significantly degrade the quality of the optical signal, the difficulty of implementing all-optical functions such as buffering and header processing have been hampering the application of optics in short-range multihop communications.

However, the recent advancements in nanophotonics, i.e. the study of the behavior of light in the nanoscale, are expected to modify this trend by enabling the design and development of nanoscale optical building blocks and its integration with standard CMOS processes. Silicon nanophotonics has been proposed as an incredibly promising monolithic integration platform of photonics and electronics for potential low cost, future high yield, simpler packaging integration of nanophotonic components and CMOS electronics [1]. A further step into nanophotonic devices has been recently reported by graphene and silicon integration showing promising properties in terms of bandwidth, energy consumption and area overhead, making them perfect candidates for applications such as on-chip networking.

In this paper, we briefly review the state-of-the-art in graphene and silicon nanophotonics (Section 2) and its utilization for on-chip communication in multicore processors (Section 3). We also propose a hybrid optical/wireless architecture for massively multicore processors, in which graphene appears as an enabler of both nanophotonics and nanoscale wireless communication (Section 4). In this architecture, the photonic NoC will transmit heavy flows of data, whereas the wireless NoC will be used for the transmission of control messages and light data flows.

2. THE ADVENT OF NANOPHOTONICS

Optical communications have delivered the best-of-class performance during the last 30 years, providing enormous capacity in terms of bandwidth and distance also providing high signal quality. High bandwidths are also required at the shortest distances, as for example chip interconnections, but conquering this communication sector requires a further development of photonic devices. Power consumption is a major concern in information processing and short distance communication, and it has been stated that the global interconnect problem will not be solved by cooper because of its bandwidth to power ratio and signal integrity limitations [2]. Photonics devices can in principle provide an energy efficient solution, especially for longer off-chip distances, but competing with electrical wires which operate at energies in the range of 1 pJ/bit requires much smaller photonic devices than the current ones. Nanophotonics has been proposed as the most promising technology for, on the

one hand, providing small footprint devices to be integrated at the chip level, and on the other hand, potentially addressing the challenging energy targets of transmitter energies of about 10 to 100 fJ/bit [3].

Several technologies are under intense research for low-energy, low drive voltages for compatibility with CMOS technology, which dominates consumer electronics [1]. Silicon material is already providing significant results. Very recently, electro-optic modulators, implementing 220 nm thickness rib waveguides have demonstrated 25Gb/s with drive voltages of less than 1V, showing a first nanophotonic device compatible with high-performance CMOS electronics [4].

2.1 Nanoscale Silicon Photonics

Silicon photonics has been focusing a very high research interest by academia and industry as the best candidate for optics and electronics integration [5] and nanoscale photonics. It is being proposed, on the one hand, for hybrid integration of a photonic active layer, e.g. III-V materials and with silicon photonic circuits as it is being worked at the FP7 HELIOS project. On the other hand, silicon is also leading to subwavelength nanophotonic structures for silicon-wire waveguides, opening a new field for engineering the refractive index of silicon waveguides [6]. Two main nanophotonic waveguides have been initially considered, commonly known as photonic wires and photonic crystals [7]. The photonics wire is a total internal reflection waveguide by means of a high index contrast and small cross section, with a typical width of 300-500 nm. The vertical confinement is obtained by deposition of the silicon waveguide on top of a silicon oxide insulator layer (SOI) [7]. The photonic crystal also achieves the vertical confinement by the same SOI technique, while the horizontal confinement is produced by a line defect in a photonic crystal structure, i.e. a periodic structure with a high refractive index contrast and a period of the order of the wavelength of the light in the material.

2.2 Graphene Nanophotonics

Graphene is another material providing outstanding properties for nanophotonics. On the one hand, graphene has demonstrated the capability to propagate strong confined light in the form of plasmons in graphene nano-structures [8]. Furthermore, a graphene p-n junction shows a strong gate-activated photoresistance [9]. First integration of graphene and silicon nanophotonics is showing highly relevant results, showing an enormous potential. A first graphene-based optical modulator has been demonstrated showing an electro-optical bandwidth of 1 GHz at a broad spectrum from 1.35 to 1.6 μm [10]. It represents a significant step towards reduced footprint devices as the modulator area is reduced to only 25 μm^2, thanks to the high absorption of graphene leading to a modulation capability of 0.1 dB/μm. At the receiver side, a graphene transistor-based photodetector at 40GHz has been demonstrated, while the analysis of the results suggests potential intrinsic bandwidths in the order of 500 GHz [11].

3. APPLICATION OF NANOSCALE PHOTONICS IN COMMUNICATIONS

Given the features of nanophotonics-enabled components in terms of performance, size and CMOS compatibility, the goodnesses of optical communications can be made extensive to short-range applications. Indeed, integrated and switched all-optical schemes can be used as device interconnections at different scales, from the cabinet level, i.e. rack-to-rack, down to the chip level, i.e. inter-core communication. The emphasis of this paper is on optical communications at the chip level.

3.1 Exascale Computing

Exascale Computing refers to computing capabilities over 10^{18} operations per second, and is considered the next big frontier in the world of high performance computing (HPC). Taking advantage of parallel computing, HPC systems are generally clusters consisting of up to hundreds of racks which contain multiple processors. How these racks will communicate, internally and between them, is therefore a critical issue. Since extremely high bit-rates and an energy consumption below the fJ/flop barrier is needed, nanophotonics seems the only way to go.

3.2 Photonic Network-on-chip

In the ever-changing field of microprocessor design, multicore architectures, i.e. the interconnection of several independent processors or cores, are currently the dominant trend for both conventional and high-performance computers. Unlike in single-core designs, the performance of multicore processors is mainly determined by the capabilities of the on-chip network that interconnects its cores, usually referred to as Network-on-Chip (NoC).

Initial NoC designs consist of wired meshes with one router per core, and therefore communication is typically multihop. However, as the number of cores per chip increases, such designs present significant challenges in terms of bandwidth, area overhead and energy consumption. Traditional wireline meshes do not scale well in average hop count, and thus in terms of latency and throughput. Other wireline configurations may improve scalability, but always at the expense of area and power, scarce resources in this scenario.

In light of the scalability problems arising from wireline NoC design, the research community has been looking for appropriate alternatives for on-chip communication. In this sense, the breakthroughs accomplished in nanophotonics have not gone unnoticed, and the employment of on-chip optical communication has been

proposed mainly due to its outstanding bandwidth and energy consumption capabilities. Precisely, the energy consumption in an optical link is independent of both the transmission distance at the chip level, and the transmission bitrate as switches change their state once per message. Such features allow the design of energy efficient network architectures that maximize the throughput by reducing the communication latency and offering extremely high bandwidth through Dense Wavelength Division Multiplex (DWDM). Furthermore, the extremely reduced size of the nanophotonic components provides a moderate area overhead.

A wide variety of photonic NoC designs can be found throughout the literature, from simple and conventional to novel and tailor-made topologies, including both arbitration-based and contention-free proposals. Table 1 shows the main characteristics of a selection of photonic NoC proposals, which can be classified as follows. On the one hand, some proposals advocate for the implementation of an all-to-all interconnection scheme through a bundle of shared waveguides [12-14]. In this case, the wavelength distribution and the bus structure determine whether arbitration is needed or not. On the other hand, both circuit-switched and packet-switched architectures can be built upon a network of optical switches [15-19]. These switches can be configured either following a fixed TDM [17] or WDM basis [15], or dynamically by means of a path setup phase previous to the data transmission [16,18].

Table 1. Implementation examples of Photonic NoCs

Name [Reference]	**Topology**	**Arbitration?**	**Hybrid?**
ATAC [12]	Full Crossbar	No	Yes
CORONA [13]	Full Crossbar	Yes (token)	No
FIREFLY [14]	Partial Crossbars	Yes (reservation)	Yes
[15]	2D-HERT	No	No
[16]	Torus	Yes (path setup)	Yes
[17]	Mesh	Yes (TDM)	Yes
IRIS [18]	Mesh	Yes (path setup)	No*
PHASTLANE [19]	Mesh	Yes (buffering)	No

** IRIS is described as hybrid, but the term does not refer to a mixture of interconnect technologies.*

4. A POTENTIAL SOLUTION FOR ON-CHIP COMMUNICATIONS

The design of scalable photonic NoC architectures is conditioned by the lack of all-optical multiport switches, routers or efficient flow control mechanisms. In fact, some current photonic NoC designs, e.g. [12,13], cannot be scaled beyond a few hundreds of nodes due to the need for all-optical arbitration schemes, or, in its absence, for often-complex contention-free architectures.

One possible solution is to adopt a hybrid approach, wherein different communication technologies can be used in different logical planes while being located in different physical planes by means of 3D stacking. That is precisely the strategy followed in [16-18], where a parallel NoC is in charge of controlling the state of the switches of a photonic mesh, either providing a path setup mechanism [16,18] or arbitrating the access to the switches on a time-multiplexing basis [17].

Even though hybrid proposals might offer better scalability results than its all-optical counterparts, the inherently rigid nature of the wireline control channel still limits the capabilities of the whole NoC, due to the following. Common and necessary operations in multicore processors such as data coherency and consistency become critical issues as the number of cores increases, since they require significant amount of on-chip communication. While these and other specific applications would greatly benefit from efficient broadcast and multicast schemes, this is not feasible by means of wireline on-chip networks.

At the UPC, N3Cat and GCO are working on a hybrid solution that aims to provide reconfigurability and broadcast and multicast capabilities by means of wireless on-chip communication, while maintaining the excellent conditions of optical communication. In our wireless-photonic hybrid NoC (see Fig. 1), the wireless channel will deal with control and light flows of information, as a support of the main photonic channel. Such wireless system enables broadcasting, multicasting and all-to-all communication, significantly alleviating the communication load resulting from data coherency, consistency and synchronization, among others. It is worth to note that although the proposal in [18] provides broadcast communication for such functions, the nature of this waveguide broadcast network is still rigid and its floorplanning difficult to scale.

Graphene, owing to its outstanding properties, is the key enabler of this hybrid approach, especially in the building up of the wireless plane. In a *Graphene-enabled Wireless Network-on-Chip* (GWNoC), graphene-based nano-antennas will be employed so as to implement wireless communication at the core level. This is possible by virtue of the extremely reduced size of the nano-antenna as well as its potential for radiating signals at the Terahertz band. While the employment of metallic on-chip antennas was considered, their area overhead and potential bandwidth are not sufficient in this bandwidth-intensive and area-constrained scenario.

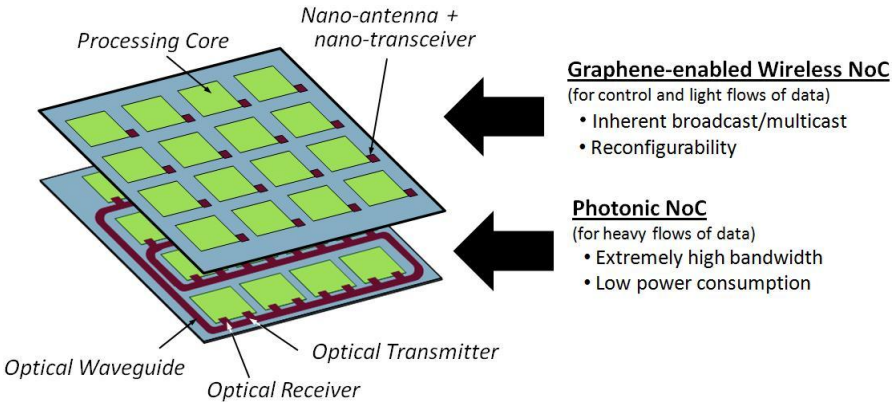

Figure 1. Example of a graphene-enabled hybrid wireless-optical NoC

5. CONCLUSIONS

The advent of nanophotonics at several technologies as silicon and graphene, opens the way for high-speed and energy efficient on-chip communications. In this paper, we performed a first overview of the state-of-the-art of nanophotonics, especially on silicon and graphene, and its application in the NoC scenario. We also discussed the need for hybrid NoC architectures and suggested a tentative approach, based on a graphene-enabled optical-wireless scheme, to address this problem.

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REFERENCES

[1] T. Baehr-Jones et al. “Myths and rumours of silicon photonics”, Nature Photonics, vol. 6, pp. 206-208, 2012.
[2] R. G. Beausoleil, et al. “Nanoelectronic and Nanophotonic Interconnect”, Proc. IEEE, vol. 96, Feb 2008.
[3] D. A. B. Miller, “Device Requirements for Optical Interconnects to Silicon Chips,” Proc. IEEE 97, 1166-1185, 2009.
[4] T. Baehr-Jones et al. Preprint at http://arxiv.org/abs/1203.0767, 2012.
[5] C. Gunn, “CMOS photonics for high-speed interconnects,” IEEE Micro, vol. 26, no. 2, pp. 58–66, 2006.
[6] P. J. Bock et al. “Subwavelength grating crossings for silicon wire waveguides”, Optics Express, vol18, pp: 16146-55, July 2010.
[7] W. Bogaerts, et al. “Nanophotonic Waveguides in Silicon-on-Insulator Fabricated With CMOS Technology”, IEEE J. Lightwave. Techn., vol. 23, pp: 401-412, Jan 2005.
[8] F. H. L. Koppens, D. E. Chang, and F. J. G. D. Abajo, “Graphene Plasmonics: A Platform for Strong Light-Matter Interactions,” Nano Letters, pp. 3370–3377, 2011.
[9] M.C. Lemme et al. “Gate-activated photoresponse in a graphene p-n junction”, Nano letters, vol. 11, no. 10, pp. 4134-7, 2011.
[10] M. Liu et al. “A graphene-based broadband optical modulator,” Nature, vol. 474, no. 7349, pp. 64-7, 2011.
[11] F. Xia et al. “Ultrafast graphene photodetector”, Nature Photonics, vol. 4, pp. 839-843, Dec 2009.
[12] G. Kurian et al. “ATAC: A 1000-Core Cache-Coherent Processor with On-Chip Optical Network,” in Proceedings of the 19th international conference on Parallel architectures and compilation techniques. ACM, 2010, pp. 477–488.
[13] D. Vantrease et al. “Corona: System implications of emerging nanophotonic technology,” ACM SIGARCH Computer Architecture News, vol. 36, no. 3, pp. 153–164, 2008.
[14] Y. Pan et al. “Firefly: Illuminating Future Network-on-Chip with Nanophotonics,” ACM SIGARCH Computer Architecture News, vol. 37, no. 3, pp. 429–40, 2009.
[15] S. Koohi, M. Abdollahi, and S. Hessabi, “All-optical wavelength-routed NoC based on a novel hierarchical topology,” in Fifth IEEE/ACM International Symposium on Networks on Chip (NoCS), Pitts, 2011, pp. 97–104.
[16] A. Shacham, K. Bergman, and L. P. Carloni, “Photonic networks-on-chip for future generations of chip multiprocessors,” IEEE Transactions on Computers, vol. 57, no. 9, pp. 1246–1260, Sep. 2008.
[17] G. Hendry et al. “Silicon nanophotonic network-on-chip using TDM arbitration,” in 2010 18th IEEE Symposium on High Performance Interconnects. IEEE, 2010, pp. 88–95.
[18] Z. Li et al. “Iris: A Hybrid Nanophotonic Network Design for High-Performance and Low-Power on-Chip Communication,” ACM Journal on Emerging Technologies in Computing Systems, vol. 7, no. 2, pp. 1-22, 2011.
[19] M. J. Cianchetti, J. C. Kerekes and D. H. Albonesi “Phastlane: a rapid transit optical routing network”, ACM SIGARCH Computer Architecture News, vol 37, no. 3 pp. 441-450, 2009.